A Novel Microwave Cross-Point Switch MMIC Employing Thyristors for Broadband Services[1]

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***Abstract* — A novel GaAs 16x16 cross-point switch MMIC is presented. The switch MMIC incorporates 256 GaAs microwave thyristor devices as the switching elements. The thyristors are two terminal devices with anodes connected to a common horizontal electrode and cathodes connected to a common vertical electrode. The bistable operation of the thyristors permits *x-y* addressing at the edge of the chip to turn on and off each thyristor. Applications include low cost, low power, high bandwidth switching of signals for broadband services. A detailed description of the thyristor device, MMIC structure and design, and simulation and experimental results are presented.**

I. INTRODUCTION

There has been considerable progress in recent years in the technology of switching multiple, high bandwidth communication channels within a telecommunication system. A core-switching element, referred to as a switch matrix, routes multiple input communication signals to multiple output transmission ports in a re-configurable manner. Whether the switch matrix is optical MEMs based or digital circuit based, common requirements include compactness, scalability, low power, switching times of less than .1 msec and high channel-channel isolation or low cross-talk. In addition, for high input/output port count, the switch matrix may be strict sense non-blocking which means, for instance, any two unused communication channels can be swapped without interruption of any other communication channels which are carrying data [1]. Typically, large port count switch matrices are constructed from smaller port count sub-switches. Examples of these are Clos and Spanke large port count switch matrices [1]. Digital based switch matrices have the additional onus of meeting high bandwidth and jitter requirements especially at OC-192 and OC-768 data rates.

This paper reports on an analog based 16x16 cross-point switch MMIC. The circuit schematic of the MMIC is shown in Fig. 1, in this case with *N* inputs and *M* outputs. Analog based means that the MMIC is composed of thyristor switch devices having a conducting (on) state and a high isolation (off) state. Broadband microwave signals are transmitted through the device in the on state with low insertion loss. In the on state, the thyristor behaves like a PIN diode in which electrons and holes flood the intrinsic GaAs layers resulting in high conductivity. In the off state, isolation is determined by the depletion layer thickness of the intrinsic GaAs layers and the resulting capacitance. The advantage of using thyristors is that on state and off state control of each device is achieved by the combination of the bistable nature of the thyristor and bias pulses applied to the upper and right side of the MMIC (see Fig. 1). For an *N*x*M* switch MMIC, there are therefore *N*+*M* control biases. The use of PIN diodes instead of thyristors would necessitate *N*x*M* bias controls connected to each PIN diode resulting in extreme circuit complexity. Since PIN diode switches have been reported to operate from DC to mm-wave frequencies near 100GHz [2], the implication is that a cross-point switch composed of thyristor devices with sufficiently low off state capacitance can effectively switch with the performance requirements mentioned above at OC-768 data rates.

II. MICROWAVE THYRISTOR DESIGN

Thyristor devices have typically been used for power switching applications for the past forty years [3]. The thyristor is characterized by a bistable operation in which the device becomes conducting when a voltage difference applied between the anode and cathode exceeds the break-over voltage. For power devices, the break-over voltage is determined by the onset of avalanching within the device. The microwave thyristor described here is composed of a p^+-i-n-i-p-n^+ GaAs epitaxial stack grown on semi-insulating substrate. Device isolation is achieved by a wet etch in which 20 μm diameter mesas are formed on a 10 mil pitch. An applied bias across the epitaxial stack results in depletion of the n-i-p junction and eventual reach through of the n-layer provided $N_d<N_a$. At this point, a reduction of the built in potential of the p+-i-n junction occurs and holes are thermionically transported to the p region of the device that behaves much like the base of a transistor. The p-n+ junction becomes forward biased at which point electrons are injected into the intrinsic layers.

[1] TeraBurst patents pending.

The device is now in a state in which more and more holes and electrons flood into the central portion of the thyristor. The potential between the anode and cathode collapses to a value comparable to the turn on voltage of a PIN diode. Silvaco BLAZE simulations show that this process takes approximately 1-2 nsec. Note that the break-over voltage is determined by the reach through voltage of the n-layer that is controlled by the doping level. The off-state device capacitance is separately controlled by the thickness of the two intrinsic layers. Fig. 2 depicts the transient process for turn on. Note that voltage pulses must be applied simultaneously to both anode and cathode to achieve turn-on. An adjacent thyristor along the same horizontal or vertical axis shown in Fig. 1 experiences a potential increase of $V_{off}+V_{bo}/2$ that is insufficient for turn on. The device is reverted to the off state by applying pulses to ground. The thyristor device was designed for an off state capacitance, C_{oj}, of 15.8 fF and the typical on state series resistance, R_s, was 5.7 Ω.

III. CROSS-POINT SWITCH OPERATION

For non-broadcast operation of the thyristor MMIC switch array, exactly one thyristor is turned on per row and corresponding column. The signal propagates along the horizontal transmission line and scatters in four directions at the thyristor that is effectively a point contact short with the vertical transmission line. Power scattered to the top and right edge of the chip (see Fig. 1) must therefore be absorbed by a 50Ω termination in order to eliminate time-delayed versions of the original signal at the output. These 50Ω terminations, currently off-chip, must also have the capacity of passing low frequency thyristor bias control pulses. This is accomplished through the design of a DC to microwave frequency bias tee that will not be discussed further in this paper. The nominal insertion loss at the output of the switch array is therefore 6dB. Any losses due to connectors, and package and PCB transmission line losses would be in addition to this. For broadband SONET signals, frequency dependent losses have the effect of eye closure and jitter. Equalizing circuitry and 3R (regeneration-reshaping-retiming) post processing can recover the signal even with 10dB frequency dependant loss from DC to the upper cutoff frequency of interest.

IV. DESIGN OF CROSS-POINT SWITCH MMIC

A. Fabrication

The MMIC has been implemented on 100-μm thick semi-insulating GaAs substrate using BCB microstrip transmission lines. A representative cross-section of the MMIC is shown in Fig. 3. After mesa isolation of the thyristor devices, a metal ground plane is deposited over the etched area with openings for the thyristor mesa. A 5-μm BCB layer that acts as the substrate for the microstrip interconnects is then spun on the wafer and cured. The BCB around the thyristor is then removed and air-bridges are fabricated to connect horizontal and vertical transmission lines to the anode and cathode of the thyristors. An overlay of BCB is then spun on and cured for passivation and to back fill the air bridges The dimensions of the die for the 16x16 and 16x32 MMICs are approximately 4.6 mm x 4.6 mm and 4.6 mm x 5.9 mm, respectively. Transmission line pitch is 250 μm (~10 mils).

B. Packaging

BGA technology has been selected to package the die since it offers low-insertion loss at mm-wave frequencies and modularity. Due to large number of RF I/O ports, laminate materials have been used to design a multilayer BGA package (see Fig. 6). Because the dimensions of the dies are relatively large compared to the thickness, a metallic carrier is first attached to the dies before placing them in the packages to prevent die cracking.

C. Design of Transmission Lines

An important feature of the MMIC design is the use of microstrip lines on BCB instead of GaAs. In other words, 5-μm BCB layer was used as substrate for the microstrip lines instead of the 100-μm thick GaAs substrate. This allowed very narrow (12-μm) 50-Ohm transmission lines that would not be possible otherwise on the top of GaAs. In fact, the combination of periodic thyristor capacitance and transmission line interconnects for any row or column of the MMIC forms an artificial transmission line. The periodic capacitance of the thyristors are absorbed by a reduction in interconnect transmission line width from 12-μm to approximately 10-μm.

A picture of the 16x16 cross-point switch MMIC is shown in Fig. 4. Note that the circuit has low-pass filter structures for each input and output as shown in Fig. 5 to compensate the wire-bond inductances. One of the ways of compensating the wire bond-inductance is to design a T-type L-C-L low-pass network where the wire-bond inductance is one of the inductive elements. The capacitive term of the network can be conveniently created by using the area under the wire-bond pad. The remaining task is to create another inductive term after the wire-bond pad. However, because the width of 50-Ohm transmission lines is already at the photolithographic limits of the process, additional means were required to create an inductive section. Therefore, it was decided to remove some portions of the ground plane at each transition to increase the inductance of the microstrip lines (see Fig. 5).

Reduced transmission interconnect line width by the use of 5-μm thick BCB substrate was also extremely crucial in the consideration of horizontal line to line and vertical line to line coupling. Far end microstrip line-to-line coupling is exacerbated by a large difference in dielectric constants between the substrate on which the microstrip resides and the overlaying dielectric constant due to an increased difference in the even- and odd-mode phase velocities. Since the dielectric constant of BCB is 2.7, the even- and odd-mode phase velocities are closely matched resulting in reduced far end coupling. On the other hand, near end coupling is reduced by the large pitch to microstrip line width ratio of 25. Simulations with ADS show that far-end coupling is –60dB up to 40GHz for two 50Ω transmission lines on BCB with 10mil pitch and 4.6mm length and near-end coupling is –70dB. It was found that the array channel-channel isolation and crosstalk is dominated by coupling through the off state thyristor capacitance.

D. Cavity Resonance Modes

Potential cavity resonance in the GaAs substrate was another important issue. As can be seen in Fig. 3, there are two ground planes on the top and bottom surface of the GaAs substrate. There are also ground via-holes along the periphery of the die to bring up the ground currents from the bottom ground plane to the ground plane of the microstrip lines. This configuration forms a rectangular cavity where resonance modes can be excited in the frequency band. Since there are ground plane openings under the inductive portion of the input and output matching networks as well as at the base of each thyristor, potential coupling between microstrip lines and the cavity formed beneath them exists. Therefore, additional GaAs substrate vias with 20 mils pitch across the whole die were fabricated thereby shorting the vertical component of electric field and suppressing any resonance mode.

V. MEASUREMENT RESULTS

To test the switch, a prototype PCB board is designed as shown in Fig. 7. GPPO connectors were used at the PCB housing to allow connection to the 16 inputs and outputs. Fig. 8 shows the resulting typical output eye diagram for a 2^{23}-1 PRBS OC-192 SONET input signal. The BER was better than 10^{-14}. The eye diagram quality can be significantly improved by the use of a 10GHz limiting amplifier from GTRAN at the PCB output. Fig. 9 shows a typical insertion loss for path (2,16), which is the second input from the top of the array and last output. Note there is a slope of 3-4dB from 0.05-12GHz that is mostly due to PCB and package trace loss. Fig. 10 shows the isolation when this path is turned off. The on/off insertion loss ratio is greater than 26 dB at 10 GHz and 40 dB at 1 GHz.

VI. CONCLUSION

A novel compact GaAs 16x16 cross-point switch MMIC utilizing microwave thyristors is presented for the first time. The pitch and size of the die is largely determined from package fabrication constraints. Further improvement in the resolution of packaging technology will permit a smaller die size. While low BER transmission of OC-192 SONET signals has been demonstrated, a further reduction of thyristor capacitance will result in a MMIC that is operational at OC-768 data rates. Although the MMIC was originally designed for optical systems, it can be used in any low-power mm-wave switching application that requires high density.

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[3] S. M. Sze, *Physics of Semiconductor Devices*, 2nd edition, New York: John Wiley & Sons, 1981.

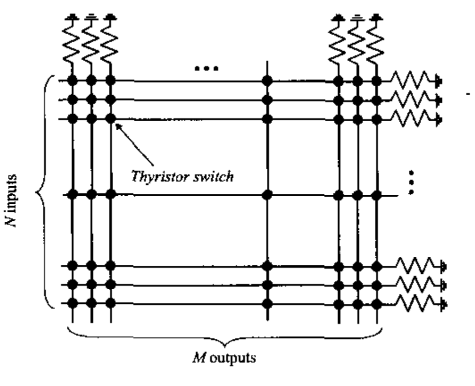

Figure 1: Equivalent circuit schematic of an *N*x*M* cross-point switch incorporating thyristor switch devices.

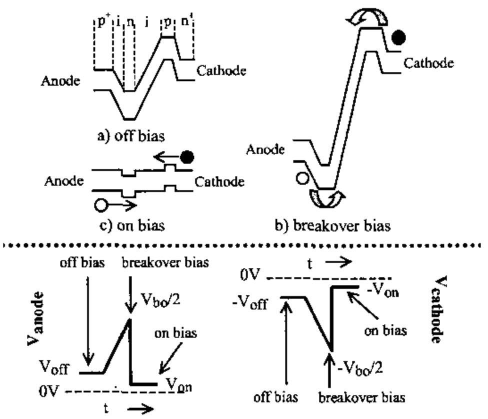

Figure 2: Band diagram (top) of microwave thyristor as the device is turned on and the anode and cathode voltages (bottom).

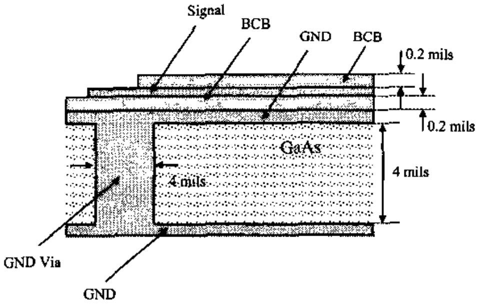

Figure 3: Representative cross-section of the GaAs switch MMIC.

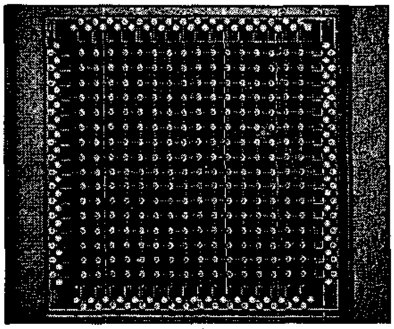

Figure 4: Picture of the 16x16 thyristor cross-point switch die. Dimensions of the die are 4.6 mm x 4.6 mm.

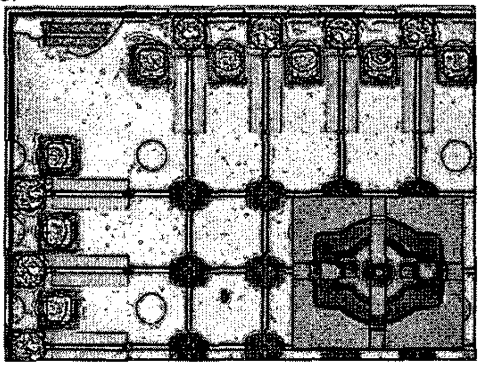

Figure 5: Pictures of the switch die showing low-pass filter networks for wire-bond compensation and junction overpass.

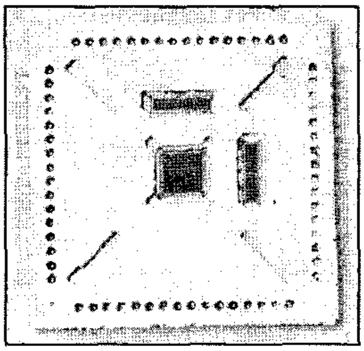

Figure 6: Picture of the 16x16 MMIC in the BGA package. The two dies on the top and right are the bias-tee circuits.

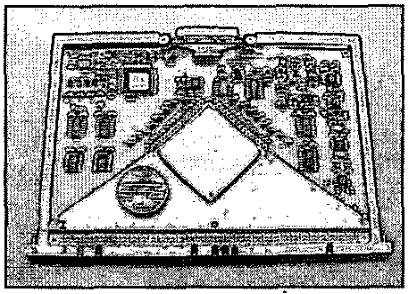

Figure 7: Picture of the manufactured PCB incorporating the packaged switch of Fig. 6.

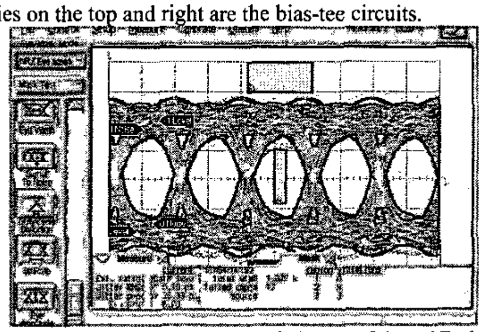

Figure 8: Output eye diagram of path (2,16) of the PCB shown in Fig. 7 (BER<10^{-14}).

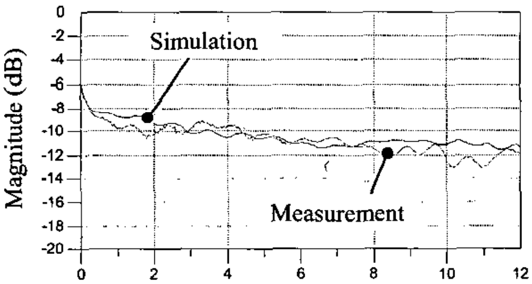

Figure 9: On insertion loss (dB) of path (2,16) of the PCB shown in Fig. 7.

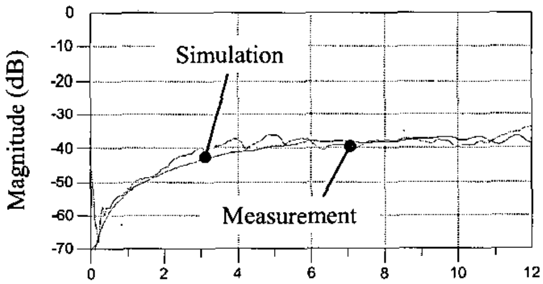

Figure 10: Off insertion loss (dB) of path (2,16) of the PCB shown in Fig. 7.